REVISIONS

REV	DESCRIPTION	DATE	APPROVED
1	SEE CHANGE ORDER 1122-01	02-08-91	DLSOLT
2	CHANGE DOC AND REF NUMBER	11-15-91	DLSOLT
3	ADD DIGITAL DELAY CKT	2-8-95	DLSOLT
4	TRACK ERR, MOVED R2201 FROM VCC	7-31-96	DLSOLT
-	Changed S1 and S2 from Dip Switch to 8x2 Header	02.12.02	JB

REFOSC TP1 U1D 74LS08 U2 74HC4040 (CLK, RST, Q1–Q12) U3C 74LS14 U3F 74LS14 U3E 74LS14 U3D 74LS14 TP2 SYNENAB U4B 74LS04 TP3 CLOCK

U4A 74LS04 U4E 74LS04 U4C 74LS04 (GND)

RN2 10K, SIP (R9 R8 R7 R6 R5 R4 R3 R2 R1 COM) +5 C1 0.1U GND

JMP1 HIGH JMP2 HIGH GND MSB U6 (A B C D, QA QB QC QD, RCO, CLK, G, D/U, LOAD, MX/MN) 74LS190 REFOSC U1A 74LS08

U7A U7B 74LS74 (D CLK PR CL Q Q)

U8A U4D TP5 70KHZCLK 74LS74 74LS04

TP4 U3A U3B 74LS14 C3 4.7U POWER-ON RESET (RISING EDGE) C4 0.1U U5A CEXT REXT/CEXT A B CLR Q Q 74LS221 RN1 10K, SIP C2 0.1U C5 0.1U U5B 74LS221

LSB S1 HEADER 8X2 MSB N0–N7 L1–L8 RFC C6–C13 0.1U B0–B7 GND

TO FRSYNANA PCB VCO BAND CNTL
L = HIGH FREQ BAND

RN3 10K, SIP B[0..7] C15 0.1U JB1 BERG3 R1 10K U1B 74LS08 Q1 2N3904 Q2 2N3904 C14 0.1U

RN4 10K, SIP C[0..7] C16 0.1U R0 R3 R4 R5 R6 C12 0.1U L17 RFC L18 RFC C18 0.1U JB2 AMPJ4

JMP 1 & 2 for 9 kHz spacing
JMP 3 & 4 for 10 kHz spacing
(to optional front panel select switch)

LSB END

RN5 10K, SIP MSB C19 0.1U U9 74LS165 (SER A–H QH CLK INH SH/LD)

U10 74LS165 N

LSB U11 74LS165 MSB START

LSB U12 74LS165 TP6 DATA

P2201 CARDEDGE
1QSIGNAL 2QSIGNAL 3QSIGNAL 4QSIGNAL
1QBARSIG 2QBARSIG 3QBARSIG 4QBARSIG
SYNSENSE R11 1K
CLOCK DATA SYNENAB SYNTHOUT TXINHIBT REFOSC LOCKENAB 70KHZCLK PAENABLE +18VDC TP24 GND VSS

LSB S2 HEADER 8X2 L9–L16 RFC C20–C27 0.1U RN6 10K, SIP C28 0.1U

U13 AD9501 (D0–D7,MSB, TRIGGER, RESET, CS, OUTPUT, RS, DAC, OFF, LATCH) C29 51P R6 1.82K R7 100K TP15 R8 1K VR1 1K EXTERNAL POT CONN JB5 BERG2

U14 AD9501 C30 51P R9 2.00K TP16 TP20 C34 1U TP21

DRIVE SIGNAL
L = FET OFF
TP17 U15 74ACT241 (1A1–2A4, 1Y1–2Y4, 1G, 2G) TP18 R10 10K
1QSIGNAL 2QSIGNAL 3QSIGNAL 4QSIGNAL
1QBARSIG 2QBARSIG 3QBARSIG 4QBARSIG

PA DRIVER

RN7 10K, SIP PUP1 PUP4 PUP5 PUP8 C31 0.1U
RN8 10K, SIP PUP10 PUP11 PUP12 PUP14 PUP15 PUP16 C32 0.1U

SYNTHOUT TP7 U16B U17B U17A 74LS74 PUP8 TP8 PUP5 TP9 PUP4 TP13 TP14 PUP1

ENABLE ACTIVE=HIGH TP12 L = ACTIVE R2 10K TP10 LOCKENAB TXINHIBT U1C 74LS08 U4F 74LS04 PAENABLE R3 10K TP11

DIVIDE BY 8

U18A U18B 74LS221 (CEXT, REXT/CEXT, A B CLR Q Q) C33 10P C35 10P PUP10 PUP11 PUP12 PUP14 PUP15 PUP16 TP19

U16A U8B 74LS74

R4 15,1W R5 15,1W L19 RFC +18VDC D1 1.5KE24C U19 LM7812 U20 LM7805 C36 4.7U C37 0.1U C38 0.1U C39 100U

C40 4.7U C41–C51 0.1U C52–C62 0.1U TP22 TP23 VDD VCC

NOTE: RESISTANCE IN OHMS, CAPACITANCE IN FARADS, INDUCTANCE IN HENRIES UNLESS OTHERWISE NOTED.

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Title: FREQUENCY SYNTHESIZER, DIGITAL PCB
Size: C | Document Number: S-112-200 | Rev: 4
Date: Thursday, November 07, 2002 | Sheet 1 of 1